Fig. 1

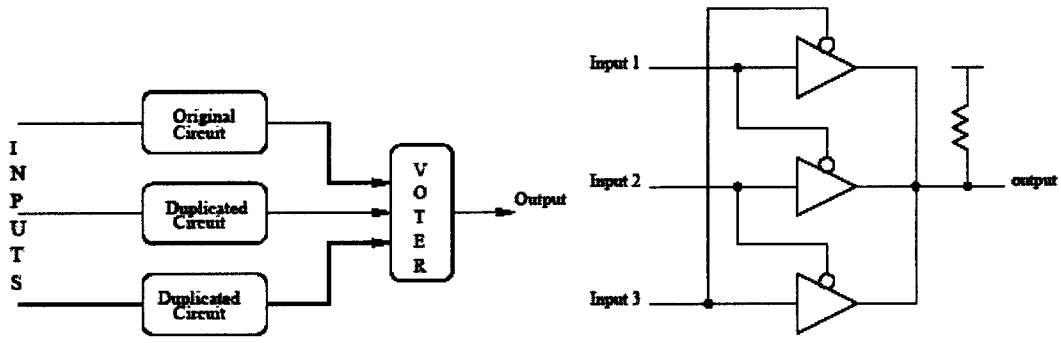

INPUTS
Original Circuit
Duplicated Circuit
Duplicated Circuit
VOTER
Output
Input 1
Input 2
Input 3
output

Fig. 2

Gate Type	P_{out}
AND	$\prod_i P_i$
NAND	1 - $\prod_i P_i$
OR	$\sum_i P_i$ - $\prod_i P_i$
NOR	1 - ($\sum_i P_i$ - $\prod_i P_i$)
XOR	$\sum_{i,j} P(i)(1 - P(j))$
XNOR	1 - ($\sum_{i,j} P(i)(1 - P(j))$)

Fig. 3

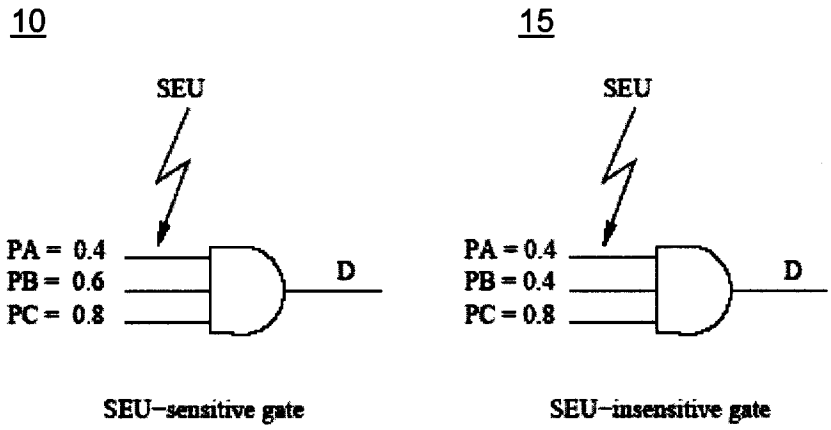

10
SEU
PA = 0.4
PB = 0.6
PC = 0.8
D
SEU-sensitive gate
15
SEU
PA = 0.4
PB = 0.4
PC = 0.8
D
SEU-insensitive gate

Fig. 4

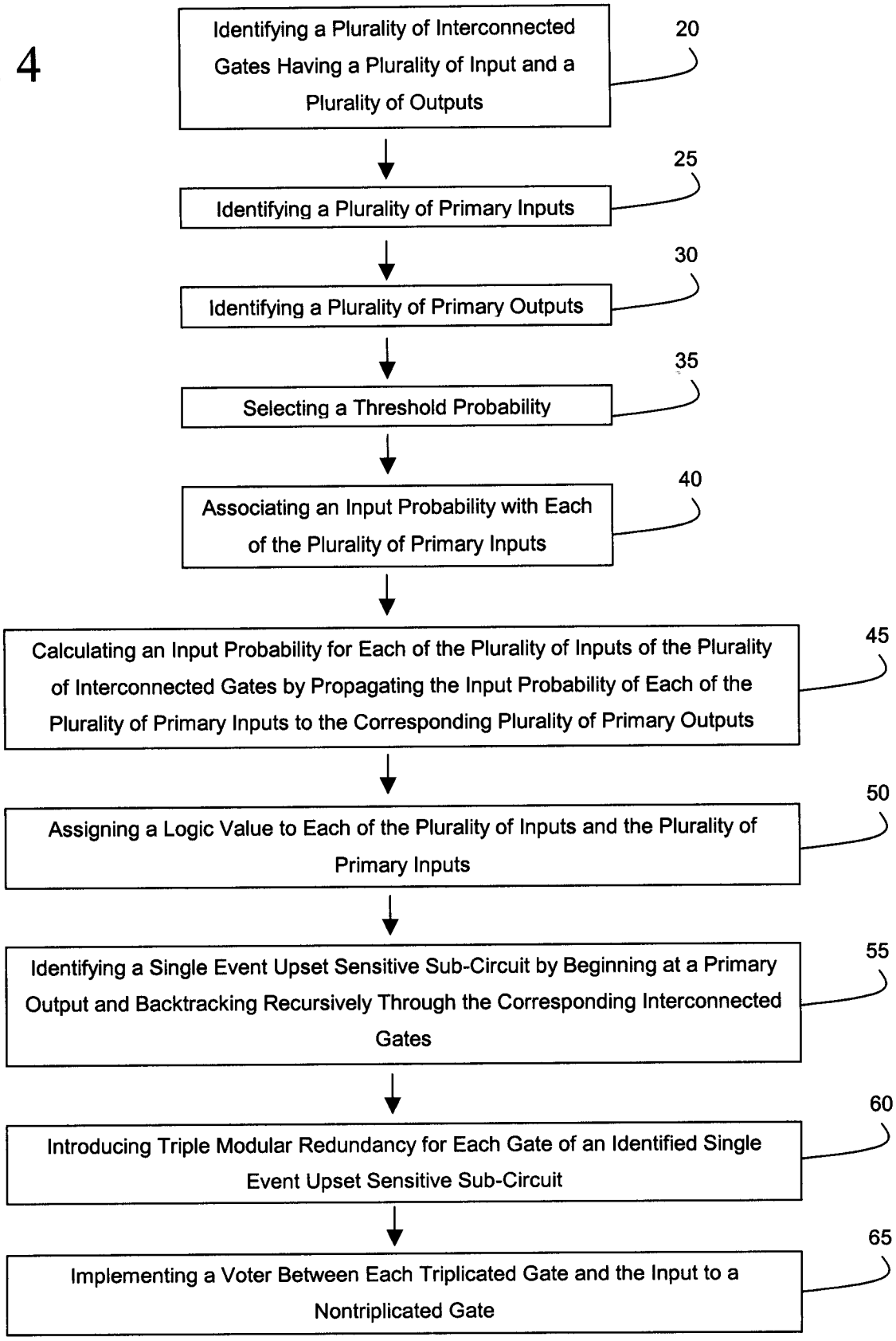

Identifying a Plurality of Interconnected Gates Having a Plurality of Input and a Plurality of Outputs
20
Identifying a Plurality of Primary Inputs
25
Identifying a Plurality of Primary Outputs
30
Selecting a Threshold Probability
35
Associating an Input Probability with Each of the Plurality of Primary Inputs
40
Calculating an Input Probability for Each of the Plurality of Inputs of the Plurality of Interconnected Gates by Propagating the Input Probability of Each of the Plurality of Primary Inputs to the Corresponding Plurality of Primary Outputs
45
Assigning a Logic Value to Each of the Plurality of Inputs and the Plurality of Primary Inputs
50
Identifying a Single Event Upset Sensitive Sub-Circuit by Beginning at a Primary Output and Backtracking Recursively Through the Corresponding Interconnected Gates
55
Introducing Triple Modular Redundancy for Each Gate of an Identified Single Event Upset Sensitive Sub-Circuit
60
Implementing a Voter Between Each Triplicated Gate and the Input to a Nontriplicated Gate
65

Fig. 5

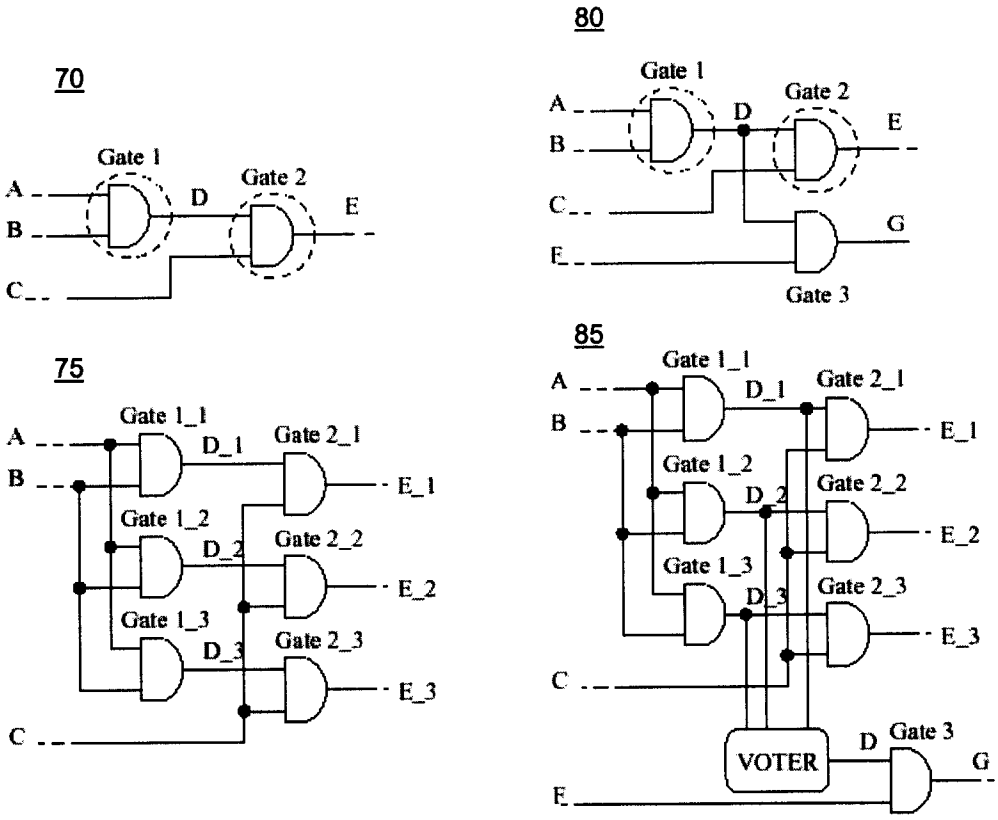
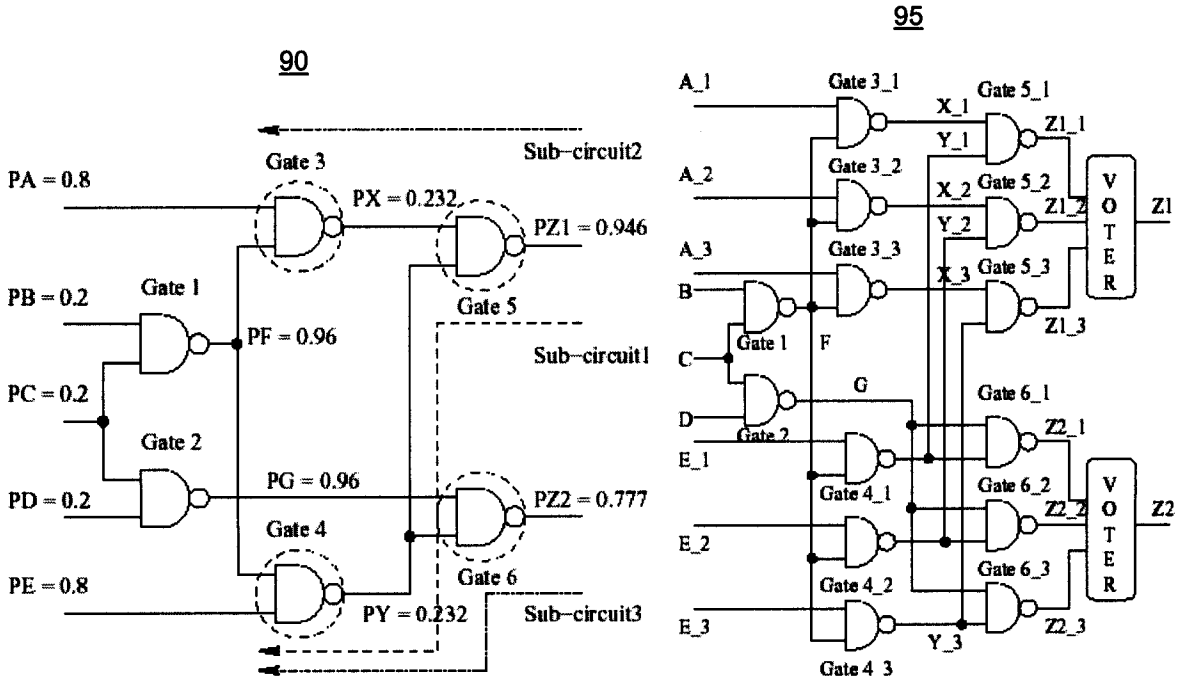

70
Gate 1
Gate 2
A
B
C
D
E
75
Gate 1_1
Gate 1_2
Gate 1_3
Gate 2_1
Gate 2_2
Gate 2_3
D_1
D_2
D_3
E_1
E_2
E_3
80
Gate 1
Gate 2
Gate 3
G
85
VOTER

Fig. 6


90
Sub-circuit2
Gate 3
PA = 0.8
PX = 0.232
PZ1 = 0.946
PB = 0.2
Gate 1
Gate 5
PF = 0.96
Sub-circuit1
PC = 0.2
Gate 2
PG = 0.96
PZ2 = 0.777
PD = 0.2
Gate 4
Gate 6
PE = 0.8
PY = 0.232
Sub-circuit3
95
A_1
Gate 3_1
Gate 5_1
X_1
Y_1
Z1_1
A_2
Gate 3_2
Gate 5_2
X_2
Y_2
Z1_2
V O T E R
Z1
A_3
Gate 3_3
Gate 5_3
X_3
Z1_3
B
Gate 1
F
C
G
Gate 6_1
D
Gate 2
Z2_1
E_1
Gate 4_1
Gate 6_2
Z2_2
V O T E R
Z2
E_2
Gate 4_2
Gate 6_3
E_3
Y_3
Z2_3
Gate 4_3